21. (Amended) The digital camera of claim 19 wherein the non-volatile memory unit is fabricated adjacent to the CMOS [imager] image sensor.

22. (Amended) The digital camera of claim 19 wherein the protective layer is fabricated as part of the CMOS [imager] image sensor.

25. (Amended) The digital camera of claim 19 wherein the CMOS [imager] image sensor comprises an active pixel array.

26. (Amended) The digital camera of claim 19 wherein the CMOS [imager] image sensor comprises a passive pixel array.

27. (Amended) A method of fabricating a CMOS imager on an integrated circuit with non-volatile memory comprising the steps of:

fabricating an array of non-volatile memory cells;

fabricating a light blocking layer over the array of non-volatile memory cells; [and]

fabricating the CMOS imager for defining an image in response to received light; and

fabricating a frame memory for storing the image from the CMOS imager.

REMARKS

Claims 1, 4-8, 11, 15, 16, 19, 21, 22, and 25-27 are amended, no claims are canceled, and no claims are added; as a result, claims 1-28 remain pending in this application.

Claims 1, 4-7, 19, 21, 22, 25, and 26 are amended to adopt a uniform phrase, namely, "CMOS image sensor" for an element. These amendments are not made for purposes of patentability and are not intended to be narrowing.

Claims 8, 11, 15, and 16 are amended to adopt a uniform phrase, namely, "non-volatile memory unit" for an element. These amendments are not made for purposes of patentability and are not intended to be narrowing.

Docket No. 703.032US1
WD # 468077

Micron Ref. No. 97-0731

Clean Version of Pending Claims

CMOS IMAGER WITH INTEGRATED NON-VOLATILE MEMORY
Applicant: Christophe J. Chevallier
Serial No.: 09/136,680

Claims 1-28, as of December 11, 2002 (date of response to first office action filed).

1. (Amended) An image sensor comprising:

a monolithic substrate;

a CMOS image sensor on the monolithic substrate and adapted for defining an image signal photoelectrically converted in response to received light;

a frame memory on the monolithic substrate and adapted for receiving the image signal from the CMOS image sensor;

an array of non-volatile memory cells on the monolithic substrate and adapted for receiving and storing the image signal from the frame memory, wherein each memory cell stores a trapped charge; and

a level of protective material fabricated over the array of non-volatile memory cells for blocking the light received by the CMOS image sensor so that the trapped charged is not erased from exposure to the light.

2. The image sensor of claim 1 wherein each memory cell is a field effect transistor with a floating gate.

3. The image sensor of claim 1 wherein the level of protective material is polyamide.

4. (Amended) The image sensor of claim 1 wherein the level of protective material is fabricated as part of the CMOS image sensor.

5. (Amended) The image sensor of claim 1 wherein the level of protective material is a layer of metal fabricated as an interconnect for electrically connecting the CMOS image sensor and other circuits on the substrate.

6. (Amended) The image sensor of claim 1 wherein the CMOS image sensor comprises an active pixel array.

7. (Amended) The image sensor of claim 1 wherein the CMOS image sensor comprises a passive pixel array.

8. (Amended) An image sensor comprising:

a single integrated circuit;

a CMOS imager in the single integrated circuit and for defining an image in response to received light;

a non-volatile memory unit in the single integrated circuit and for storing the image, wherein the non-volatile memory unit is fabricated adjacent to the CMOS imager; and

a level of protective material fabricated over the non-volatile memory unit for blocking the light received by the CMOS imager.

9. The image sensor of claim 8 wherein the level of protective material is fabricated as part of the CMOS imager.

10. The image sensor of claim 8 further comprising a micro-controller for controlling transfer of the image from the CMOS imager to the non-volatile memory unit.

11. (Amended) The image sensor of claim 10 wherein the non-volatile memory unit stores program code information for controlling the microcontroller.

12. The image sensor of claim 8 further comprising a digital signal processor for receiving and processing the image from the CMOS imager.

13. The image sensor of claim 8 wherein the level of protective material is a layer of metal.

14. The image sensor of claim 8 wherein the layer of metal is fabricated as an interconnect for electrically connecting the CMOS imager and other circuits on the substrate.

15. (Amended) An image sensor comprising:

a single integrated circuit;

a CMOS imager in the single integrated circuit and for defining an image in response to received light;

a microcontroller in the single integrated circuit and for controlling the CMOS imager;

a non-volatile memory unit in the single integrated circuit and fabricated adjacent to the CMOS imager for storing program code or data; and

a level of protective material fabricated over the non-volatile memory unit for blocking the light received by the CMOS imager.

16. (Amended) The image sensor of claim 15 wherein the non-volatile memory unit receives and stores the image.

17. The image sensor of claim 15 wherein the level of protective material is metal fabricated as an interconnect layer for electrically connecting other circuits on the single integrated circuit.

18. The image sensor of claim 15 further comprising a digital signal processor for receiving and processing the image from the CMOS imager.

19. (Amended) A digital camera comprising:

a single integrated circuit;

a CMOS image sensor in the single integrated circuit and for defining an analog image signal photoelectrically converted in response to received light;

an analog to digital convertor in the single integrated circuit and for receiving and converting the analog image signal into a digital image signal;

a frame memory in the single integrated circuit and for recording the digital image signal;

a data compression/decompression unit in the single integrated circuit and for compressing the digital image signal provided by the frame memory;

a non-volatile memory unit in the single integrated circuit and for receiving the compressed digital image signal, wherein a layer of protective material is fabricated over the non-volatile memory unit for blocking the light received by the CMOS image sensor; and

a microcontroller in the single integrated circuit and for controlling the exchange of the digital image signal between the frame memory and the non-volatile memory unit.

20. The digital camera of claim 19 further comprising:

a digital signal processor for receiving and processing the digital image signal from the frame memory;

a digital to analog convertor for converting the digital image signal to an analog image signal, wherein the digital signal processor and the digital to analog convertor are fabricated on the single integrated circuit; and

an electronic view finder for viewing the image.

21. (Amended) The digital camera of claim 19 wherein the non-volatile memory unit is fabricated adjacent to the CMOS image sensor.

22. (Amended) The digital camera of claim 19 wherein the protective layer is fabricated as part of the CMOS image sensor.

23. The digital camera of claim 19 wherein the non-volatile memory unit stores program code information for controlling the microcontroller.

24. The digital camera of claim 19 wherein the protective layer is fabricated as a metal interconnect layer for electrically connecting circuits on the integrated circuit.

25. (Amended) The digital camera of claim 19 wherein the CMOS image sensor comprises an active pixel array.

26. (Amended) The digital camera of claim 19 wherein the CMOS image sensor comprises a passive pixel array.

27. (Amended) A method of fabricating a CMOS imager on an integrated circuit with non-volatile memory comprising the steps of:

fabricating an array of non-volatile memory cells;

fabricating a light blocking layer over the array of non-volatile memory cells;

fabricating the CMOS imager for defining an image in response to received light; and

fabricating a frame memory for storing the image from the CMOS imager.

28. The method of claim 27 wherein the light blocking layer is a metal layer used as an interconnect for electrically connecting other circuits on the integrated circuit.

Claim 27 is amended to clarify the antecedent basis of an element. This amendment is not made for purposes of patentability and is not intended to be narrowing.

Antecedent basis for the "single integrated circuit" in claim 17 is now found in parent claim 15.

Withdrawal of all of the claim objections is requested.

Drawing Objections

The Office Action objects to the drawings because of the informalities addressed below: (a) In figure 1, element "memory comp/decomp 32: should be changed to --comp/decomp 32–; and (b) In figure 1, there is no connection between comp/decomp 32 and memory 34. It should include an arrow to indicate the compressed image data is fed to memory 34 as disclosed in the specification, page 6, line 20. Applicant proposes amending Fig. 1 to remove the term "memory" from comp/decomp 32 as suggested by the examiner. Approval of the proposed drawing amendment is requested.

With respect to the assertion (item "b" above), applicant respectfully traverses. Data bus 52 provides a connection between comp/decomp 32 and memory 34. See specification page 8, lines 4-5 and fig. 1. Withdrawal of the objection is requested.

Specification Objection

The disclosure is objected to because of the following informalities. In the specification, page 10, (lines 16, 28, and 29), page 11 (lines 2, 5-6, 8), all disclose "substrate 110." However, there is no disclosure of substrate 110 in figures 1-3. Applicant herein amends Figure 3 to include the substrate as described in the specification. It is believed that no new matter is proposed and the substrate is supported per 35 U.S.C. §112 in the specification. As the substrate is now included in Figure 3, withdrawal of the specification objection is requested.

§112 Rejection of the Claims

Claim 17 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant traverses. Claim 17, as originally filed, is believed to meet the requirements of 35 U.S.C. § 112, second paragraph.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§103 Rejection of the Claims

Claims 1, 4-6, 8-25, and 27-28 were rejected under 35 USC § 103(a) as being unpatentable over Schmidt (U.S. 6,278,481) in view of Zhou et al.(U.S. 5,909,026). Applicant traverses.

Claim 1 includes a monolithic substrate on which is a CMOS image sensor, a frame memory, and an array of non-volatile memory cells. Applicant can not find where Schmidt or Zhou, either alone or in combination, teach such a monolithic substrate. Moreover, Schmidt teaches away from the present invention as defined by claim 1 as Schmidt teaches a circuit board 230 that includes imager 220, lens 232 and memory 228. Applicant can not find where Schmidt or Zhou, either alone or in combination, teach a level of protective material on the array of non-volatile memory cells as recited in claim 1. Zhou merely teaches using metal II as a light shield for the frame memory array. As Schmidt and Zhou do not teach all of the elements of claim 1 and Schmidt teaches away from claim 1, applicant requests allowance of claims 1 and 4-6.

Applicant further traverses the rejection of claim 1 based on a lack of a motivation to combine Zhou with Schmidt. The Office Action states that the motivation would be increasing image quality. Applicant does not understand how providing a lelvel of protective material on

the array of non-volatile memory cells increases image quality. Image quality from CMOS imagers. Attached is a printout from a Kodak web page (http://www.kodak.com/US/en/digital/dlc/book3/chapter1/digFund4.shtml). This page states that image quality is determined by spacial resolution and brightness resolution. Applicant is unclear how increasing image quality relates to modifying Schmidt with Zhou. Specifically, applicant requests clarification how image quality would be increased. Applicant requests that the rejection of claim 1 be withdrawn due to a lack of a motivation to combine Schmidt and Zhou.

Claim 8 includes, in part, a single integrated circuit; a CMOS imager in the single integrated circuit; a non-volatile memory unit in the single integrated circuit; and a level of protective material fabricated over the non-volatile memory unit for blocking the light received by the CMOS imager. Applicant can not find where Schmidt or Zhou, either alone or in combination, teach such a single integrated circuit. Moreover, Schmidt teaches away from the present invention as defined by claim 1 as Schmidt teaches a circuit board 230 that includes imager 220, lens 232 and memory 228. Applicant can not find where Schmidt or Zhou, either alone or in combination, teach a level of protective material on the array of non-volatile memory cells as recited in claim 8. Zhou merely teaches using metal II as a light shield for the frame memory array. As Schmidt and Zhou do not teach all of the elements of claim 8 and Schmidt teaches away from claim 8, applicant requests allowance of claims 8 and 9-14.

Moreover, there is a lack of motivation to combine Schmidt and Zhou to reject claim 8 that is substantially the same as stated above with regard to claim 1 Applicant requests that the rejection of claim 8 be withdrawn due to a lack of a motivation to combine Schmidt and Zhou.

Claims 15-25 and 27-28 are believed to be allowable for substantially similar reasons as stated above with regard to claim 8. Allowance of claims 15-25 and 27-28 is requested.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmidt (U.S. 6,278,481) in view of Zhou et al.(U.S. 5,909,026) further in view of Komori et al. (U.S. 6,255,690). Applicant traverses. Claim 2 is believed to be allowable with its parent claim 1. Applicant can not find where Komori teaches the missing elements not found in Schmidt or Zhou as stated above. Allowance of claim 2 is requested.

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmidt (U.S. 6,278,481) in view of Zhou et al.(U.S. 5,909,026) further in view of Ross (U.S. 5,241,412). Applicant traverses. Claim 3 is believed to be allowable with its parent claim 1. Applicant can not find where Ross teaches the missing elements not found in Schmidt or Zhou as stated above. Allowance of claim 3 is requested.

Clams 7 and 26 were rejected under 35 USC § 103(a) as being unpatentable over Schmidt (U.S. 6,278,481) in view of Zhou et al.(U.S. 5,909,026) further in view of Kempainen (CMOS Image Sensors: ECLIPSING CCDs in Visual Information?, www.ednmag.com, October 9, 1997). Applicant traverses. Claim 7 is believed to be allowable at least because it depends from claim 1.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-349-9587) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

CHRISTOPHE J. CHEVALLIER

By their Representatives,

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Date 11 Dec 2002 By _____
Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 11th day of December, 2002.

Name Amy Moriarty

Signature _____

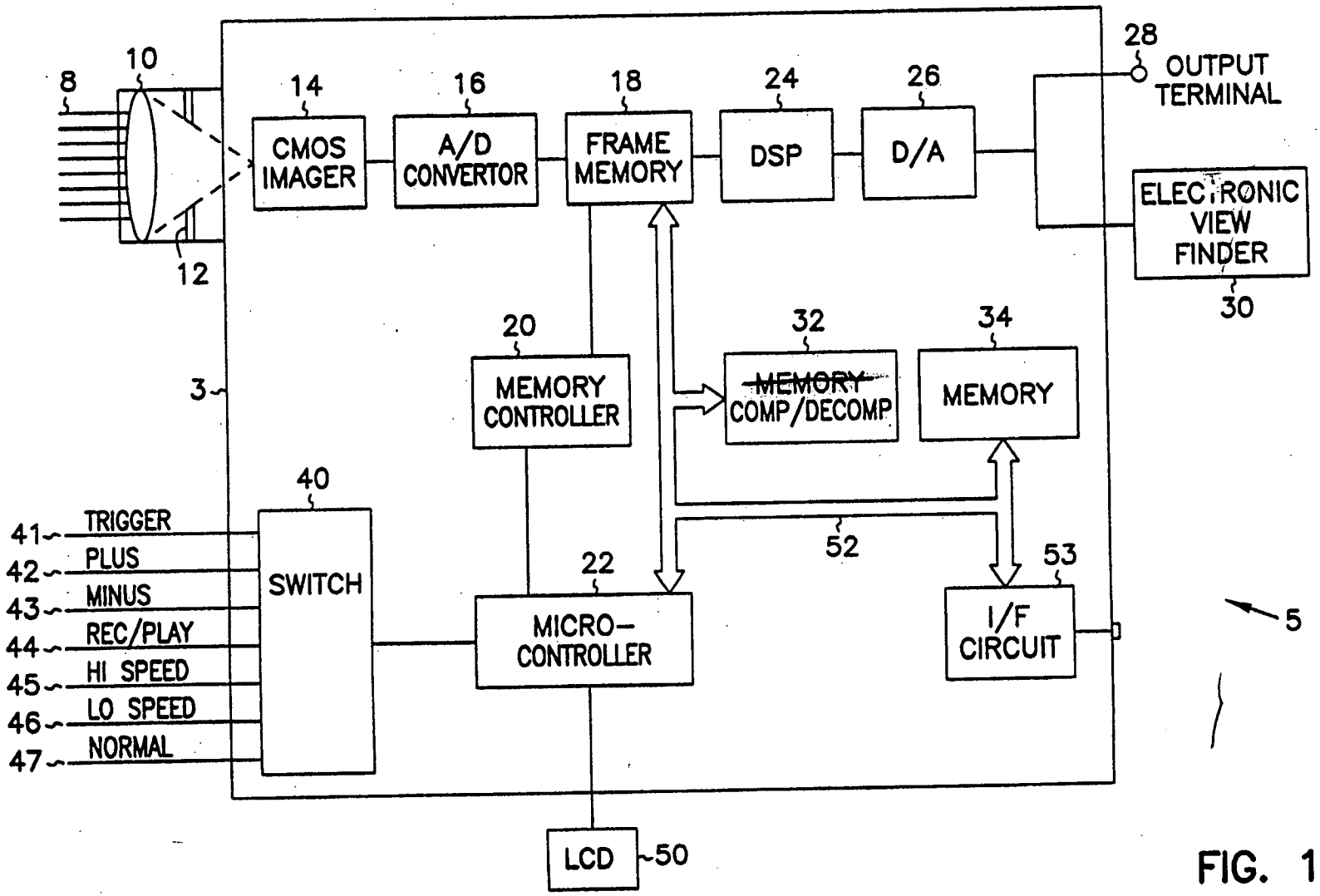

FIG. 1

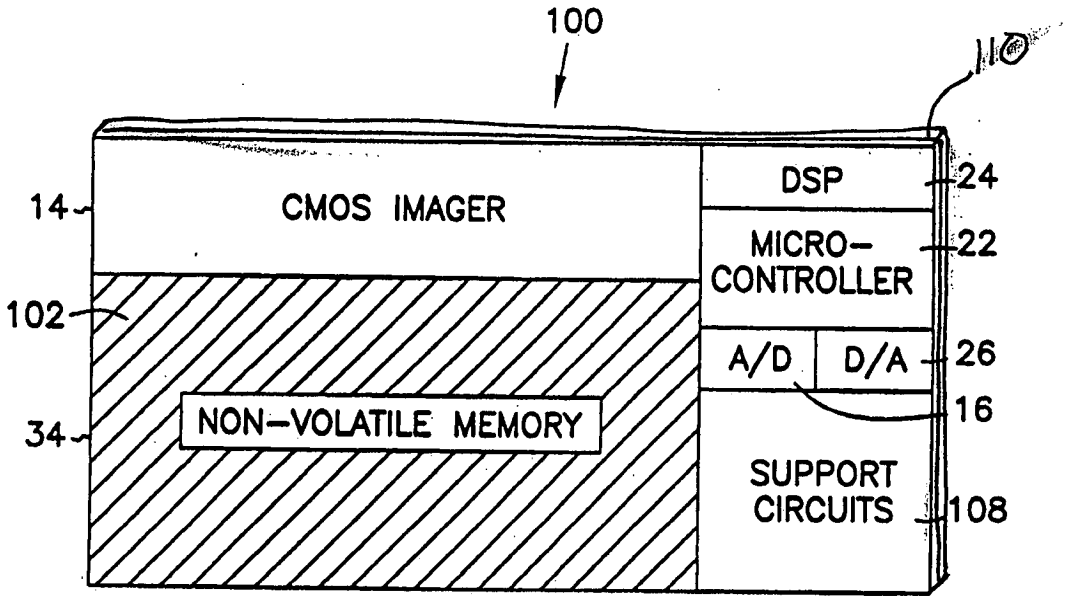

FIG. 3